Remarks

Claims 1-11 were presented for examination, and claims 1-11 were rejected in the Office Action dated June 28, 2005. New claims 12-22 have been presented herein that correspond substantially to claims 1-11 being rewritten in apparatus format. No new matter has been added.

Objection to the Specification

The Examiner objected to the specification as having informalities in paragraphs [0007] and [0010]. Amended paragraphs [0007] and [0010] have been amended herein to correct typographical errors contained therein. No new matter has been added.

Claim Rejections - §103

The Examiner rejected claims 1-11 under 35 U.S.C. § 103(a) as being unpatentable over the patent to Ishizuka (5,262,873).

Contrary to the Examiner's assertion, the patent to Ishizuka does not teach, disclose, or suggest *"extracting **only a plurality of last bits** of the first correction digital signal"* as recited in independent claims 1 and 12. Furthermore, Ishizuka does not teach, disclosure, or suggest *"extracting **only a plurality of first bits** of the second correction digital signal"* as recited in independent claims 1 and 12.

In support of the rejection, the Examiner stated that:

> From the above disclosure, by Ishizuka it is clear that after white digital correction signal is obtained, the number of bits representing the white digital correction signal are reduced with respect to the small memory size and examiner asserts that based on the teachings of Ishizuka, it would have been obvious for one of ordinary skill in the art at the time of invention was made to consider it as a matter of selecting either first few bits or last few bits from the digital correction signal because the value representing the difference is small with respect to the number of bits of the output of the A/D converter (col. 4, lines 43-52). (Emphasis added).

However, contrary to the Examiner's assertion, the limitations corresponding to selecting either first few bits or last few bits from the digital correction signal simply are not found

in the patent to Ishizuka. The Examiner is kindly reminded that, in order to establish a *prima facie* showing of obviousness, the:

> Prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP §§ 2142, 2143.

Therefore, it is impermissible for the Examiner add the limitations of the Applicant's claims into the cited reference when the cited reference does not in fact teach or suggest those limitations. The Examiner is kindly reminded that, in establishing a *prima facie* obviousness rejection:

> Knowledge of applicant's disclosure must be put aside in reaching this determination . . . MPEP § 2142.

It should be noted that the embodiment of Ishizuka cited by the Examiner is:

> . . . directed to compression of correction data which is achieved by storing only a difference between the adjacent pixels in a correction data storage means. (Col. 3, lines 28-31 "First Embodiment").

Thus, since the Examiner merely repeated the limitations of the Applicant's claims in stating the rationale for the rejection, rather than pointing to the existence of those limitations in the Ishizuka reference, which the Applicant asserts do not exist in said patent to Ishizuka, it appears the Examiner did not put aside knowledge of the Applicant's disclosure when developing the obviousness rejection. Again, the Examiner is kindly reminded that *the prior art reference* must teach or suggest the claim limitation, and such teaching or suggestion much not come from the not the Examiner based on a reading of the Applicant's disclosure and/or claims. Thus, it is respectfully submitted that the Examiner has mixed the first requirement of establishing *prima facie* obviousness, teaching or suggesting all the claim limitations, with the second requirement of establishing *prima facie* obviousness, motivation to modify a cited reference to arrive at the claimed invention. Regardless of any motivation, the cited reference must teach or suggest all of the claim limitations. Here, the patent to Ishizuka simply does not teach or

suggest the claim limitations of *"extracting **only a plurality of last bits** of the first correction digital signal"* and *"extracting **only a plurality of first bits** of the second correction digital signal"*, so a *prima facie* case of obviousness was not established. As a result, the rejection should be withdrawn.

Furthermore, it is respectfully submitted that the Examiner has failed to consider the claims as a whole. The patent to Ishizuka does not teach or suggest *"obtaining a first correction digital signal"* and *"obtaining a second correction digital signal"*, in combination as recited in independent claims 1 and 12. The Examiner is kindly reminded that when establishing a *prima facie* case of obviousness, the Examiner:

> . . . must evaluate the "subject matter as a whole" of the invention. MPEP § 2142.

Thus, since the Examiner did not establish that Ishizuka teaches or suggests claim 1 as a whole, a *prima facie* case of obviousness was not established, and the rejection should be withdrawn.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

Invitation for a Telephone Interview

The Examiner is invited to call the undersigned attorney, Kenneth J. Cool, at (720) 227-9445 if there remains any issue with allowance.

Respectfully submitted,

ATTORNEY FOR ASSIGNEE

Date: 9/23/05

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